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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,597	08/04/2003	Uri Cummings	FULCP009	6534

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,597	CUMMINGS ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,15,18,27 and 31-37* is/are rejected.

7)☒ Claim(s) *2-14, 16-17, 19-26 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 12 is objected to because of the following informalities: in line 1, "claim11" should be changed to -- claim 11 --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 15, 18, 27 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abu-Lebdeh et al. U.S. Patent 6,546,451 B1.

Regarding claim 1, Abu-Lebdeh et al. invention relates to computer buses, and in particular, to a PCI bus switch architecture used in computer systems. In column 3 line 46 through column 4 line 3, Abu-Lebdeh et al. discloses in figure 2 PCI bus switch architecture 200 comprising a plurality of PCI port controllers 210A-G and a crossbar switch 230.

Each of PCI port controllers 210A-F is coupled to a single logic device or a plurality of logic devices through respective local PCI buses, see column 3 lines 59-67. In column 4 lines 33-46, Abu-Lebdeh et al. teaches that port controllers 210A-G can operate at speeds independent of each other to accommodate different throughput

requirements. Because each logic device is coupled to one of PCI port controllers 210A-F through local PCI buses, each logic device can run at different data rate independent of each other. Each data rate has an associated clock domain as appreciated by one of ordinary skill in the art. As known in the art, buses in computer system are synchronous, and devices coupled to buses operate in synchronous mode. Hence, logic devices as taught by Abu-Lebdeh et al. are synchronous devices, which correspond to the claimed plurality of synchronous modules.

Abu-Lebdeh et al. does not expressly teach a plurality of clock domain converters, each clock domain converter being coupled to a corresponding one of the synchronous modules as claimed in the patent application. As discussed above, each of port controllers interfaces one or more logic devices, and each port controller operates at speeds independent of each other to accommodate different throughput requirements from the logic devices. As further shown in figure 5, see column 4 lines 47-64, each port controller 510 coupled to a PCI bus on one side and a port of crossbar switch 530 on the other side. The port controller performs all the PCI standard functions such as initiator and target handshaking, crossbar switch connection requesting, and traffic transaction queuing. Crossbar switch 530 provides interconnectivity between port controllers 510, and selectively routes traffic from any port controller to any other port controller. The clock speed of crossbar switch can be independent of port clock speeds, see column 10 line 61 through column 11 line 5. Due to different clock speeds between crossbar switch and port controller, crossbar switch 530 operates in asynchronous domain, and transmission of data through crossbar switch 530 between port controllers

510 is according to the asynchronous handshake protocol as appreciated by one of ordinary skill in the art. In view of the foregoing teachings, because the port controller can accommodate different throughput requirements of the logic device having the associated clock domain through a crossbar switch 530 having the associated asynchronous domain, it would have been obvious for one of ordinary skill the art that each port controller 510, taught by Abu-Lebdeh et al., performs equivalent function of the claimed clock domain converter to convert data between the clock domain of the logic device to an asynchronous clock domain of crossbar switch 530. Due to the asynchronous clock domain of cross switch 530, port controllers 510 perform target handshaking, as recited above, according to the asynchronous handshake protocol.

As recited above, crossbar switch 530, corresponding to the claimed asynchronous crossbar, is coupled to port controllers 510, which perform equivalent function of clock domain converters as claimed in the pending application. Abu-Lebdeh et al. does not teach the crossbar switch 530 implementing a first-in-first-out (FIFO) channel between any two of the clock domain converters as claimed in the pending application. However, as disclosed in column 10 line 61 through column 11 line 5, PCI bus switch 202 (including crossbar switch 230, and port controllers 210A-210G) as shown in figure 2 is preferably programmable with respect to port selection priority schemes. FIFO is known used in data communications. It is a buffering scheme in which data that enters the buffer first is also transferred out first. Hence, any port controller, which performs crossbar switch connection requesting first, can be selected first by the crossbar switch to route traffic to the requested destination as part of a port

selection priority schemes. That is equivalent to the FIFO buffering scheme. In view of the foregoing reasoning, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the crossbar switch 230, as taught by Abu-Lebdeh et al. teachings, as shown in figure 2 can be programmed to implement a FIFO (a first-in-first out) channel as part of the port selection priority schemes, between any two port controllers to facilitate communication between any two of the synchronous logic devices as claimed in the pending patent application.

Regarding claim 15, as discussed in claim 1, the crossbar switch 230 implements a FIFO channel between any two-port controllers. Because of the FIFO scheme, the asynchronous handshaking is not sensitive of any delay as claimed in the pending application.

Regarding claim 18, as disclosed in column 4 lines 61-64, crossbar switch 530 as shown in figure 5, provides interconnectivity between port controllers 510, and arbitrates between concurrent requests to the same port controller 510, coupled to a logical device.

Regarding claim 27, as disclosed in column 10 lines 22-38, figure 19 illustrates a data processing system 1900 in which a PCI bus switch can be used. According to Abu-Lebdeh et al. teachings, the data processing system 1900 includes *one or more* a CPU 1901, memory 1903, peripheral devices 1909, I/O circuitry 1905, and programmable

logic devices (PLD). Figure 19 does not show a memory controller as claimed in the pending application. Nevertheless, since the data processing system 1900 includes programmable logic devices, it would have been obvious for one of ordinary skill in the art that one of the programmable logic devices is a memory controller.

Regarding claim 31, Abu-Lebdeh et al. does not teach the PCI bus switch architecture implemented on a CMOS integrated circuit. Nevertheless, CMOS integrated circuit is well known in the art, and has known advantages. In view of that, one of ordinary skill in the art would have been motivated to implement the PCI bus switch architecture as taught by Abu-Lebdeh et al. on a CMOS integrated circuit.

3. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abu-Lebdeh et al. U.S. Patent 6,546,451 B1 as applied to claim 1 above, and further in view of Butts et al. U.S. Patent 6,002,861.

Regarding claim 32, Abu-Lebdeh et al. does not teach a computer-readable medium having data structures stored representative of the computer-bus switch architecture. However, as well known in the art of digital logic network design, one performs simulation of functional circuit design before actually building the digital logic network permanently. Butts et al. discusses such simulation in another US patent, wherein a method is disclosed for performing simulation of functional circuit design using a hardware and software emulation system. As disclosed in the abstract, Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable interconnect, which comprises a partial crossbar.

The reconfigurable interconnect permits the digital network realized on the interconnected chips to be changed at will. Since Butts et al. teachings are in the same field of endeavor, and utilizes same components (e.g. logic chips, reconfigurable crossbar, ...) to simulate a digital network in the design, one of ordinary skill in the art would have been motivated to implement computer instructions stored a computer readable medium as data structures to simulate the computer-bus switch architecture, taught by Abu-Lebdeh et al., as part of the preliminary design before actually building it permanently.

Regarding claim 33, said claim is rejected on the same ground as for claim 32 because the claimed simulatable representation is discussed in claim 32.

Regarding claim 34, figure 43 in Butts et al. invention illustrates a block diagram of a Realizer design conversion system including netlists for logic chips. The Realizer design conversion system is part of hardware and software emulation system taught in Butts et al. invention.

Regarding claim 35, as recited in claim 32, Butts et al. discloses a method for performing simulation of a digital logic network as part of design using a hardware and software emulation system. In view of that, it would have been obvious for one of ordinary skill in the art that the data structures as part of the hardware and software

emulation system can be implemented to include code description representative of the computer-bus switch architecture taught by Abu-Lebdeh et al..

Regarding claim 36, using analogous argument as for claim 35, the code description would correspond to a hardware description language as part of the hardware and software emulation system.

Regarding claim 37, as discussed in claim 32, Since Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable crossbar, corresponding to the claimed set of semiconductor processing masks, it would have been obvious for one of ordinary skill in the art that the logic chips and reconfigurable crossbar as taught by Butts et al. can be implemented to represent the computer-bus switch architecture in Abu-Lebdeh et al. invention.

Allowable Subject Matter

4. Claims 2-14, 16-17, 19-26 and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wicki et al. U.S. Patent 5,838,684 discloses "Low Latency, High Clock Frequency Plesio-asynchronous Packet-based Crossbar Switching Chip System and Method".

Venkataraman et al. U.S. Patent 6,546,451 discloses "Method and Apparatus for Decoupling Processor Speed from Memory Subsystem Speed in a Node Controller".

Nishtala et al. U.S. Patent 6,101,565 discloses "System for Multisized Bus Coupling in a Packet-Switched Computer System".

Coleman et al. U.S. Patent 5,517,662 discloses "Multiprocessor with Distributed Memory".

Snyder et al. U.S. Patent 6,760,870 B1 discloses "Algorithm for Resynchronizing a Bit-Sliced Crossbar".

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

M. Ghayour

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER